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Synchronising Circuit

FIELD OF THE INVENTION

[0001] The present invention relates to the detection of the phase of one or more data streams and more particularly to the generation of an approximation to the phase during a period when there are no data transitions in the data stream.

BACKGROUND OF THE INVENTION

[0002] Figure 1 shows a differential driver 1 that takes a differential input on conductors 2 and 3 and converts that input into a serial data stream on an output conductor 4.

[0003] It is known to use the differential driver 1 of Figure 1 as an input stage to a digital system. It is also known to generate a clock signal for the digital system from the data stream on the output 4 of the differential driver 1.

[0004] Figure 2 shows a single data stream and an associated clock signal. The clock signal shown in Figure 2 samples the data on both the rising and falling clock edges and the clock transitions are closely aligned with the mid-point of data transitions. Such alignment is preferable as the data is given the maximum time both before and after the clock transition in which to be stable. This gives the best chance of the set-up and hold times of subsequent circuits not being violated.

[0005] One method of achieving such clock alignment uses the circuit of Figure 3. A phase locked loop (PLL) 5 is shown with an input 7 receiving a reference clock signal at the required frequency. The PLL generates a number of clock outputs 8 (8 in the example of Figure 3) each at a difference phase (spaced apart by 45 degrees in the example of Figure 3). The clock signal can be placed close to the mid-point of the data transitions by selecting the most appropriate clock signal from the output 8 of the PLL 7.

[0006] Another method of determining the optimum clock signal is demonstrated with reference to Figures 4 and 5. Figure 4 shows a phase wheel with 8 phase signals indicated, representing the eight phases of the PLL output 8. Those phase signals are plotted at 0, 45, 90, 135, 180, 225, 270 and 315 degrees respectively. The phase of a data stream relative to a reference signal (for example, relative to the reference clock input) can be plotted on the phase wheel. Once the phase of the data stream is "plotted" on the wheel, the outputs 8 of the PLL that are located either side of the data stream can be identified.

[0007] Figure 5 is a block diagram of a circuit for generating the appropriate clock signal. The output of the differential driver 1 is passed to a phase detector 9 that determines the phase of the data (for example, with reference to the generated clock signal). The output of the phase detector 9 is passed to a phase interpolator 10 along with the eight clock signals from the PLL 7. A clock signal is generated by identifying the two phase signals from the PLL 5 between which the phase of the data stream falls and using the phase interpolator to generate a clock signal with a phase between those two clock signals. In the example of Figure 5, the output of phase interpolator 10 is fed back to an input of the phase detector 9. The phase detector 9 is thus used to determine the difference in the phase at the output of the phase interpolator and the phase of the data stream in the data channel. A typical phase interpolator may generate the most appropriate clock phase between those phase inputs from 16 possibilities. Thus the phase wheel can be divided into 16x8 (i.e. 128) clock phases.

[0008] The purpose of generating a local clock signal for each data channel is to ensure that each clock signal is optimised for that channel. This is particularly significant when the relative delays in the channels are not constant. Such a system is used, for example, when it is not acceptable to simply select a single clock and to use that for all data channels.

[0009] Thus in a system where each data channel is likely to have a different phase, the generation of a local clock for each data channel is advantageous. This requires the phase of the data for each channel to be identified. The more frequently the data signal of any given channel changes (i.e. has edges), the more accurately the relative phase of the data in that channel can be determined. The inventors have noted, however, that if the data signal is static (i.e. there are no data transitions for a significant period of time) then it is not possible to determine the phase of that data channel. One option for handling such a situation is to retain the previous phase value until another data transition occurs. However, this suffers from the disadvantage that actual phase of the data in the channel can become significantly different to the phase value of the local clock.

SUMMARY OF THE INVENTION

[00010] The present invention uses, in one embodiment, a clock signal, available in some applications, on one of the data channels (the "clock channel"). That channel therefore has periodic data transitions. The phase of the clock channel can be readily determined and plotted on a phase wheel such as that of Figure 4.

[00011] Although each data channel generally contains data with a different phase, the inventors have realised that in many applications, the phases of the channels will be similar, undergoing common jitter, but subject to small, possibly random, variations with respect to one another. Thus, whilst the phase of a data stream is most accurately determined from the data in that data stream, a reasonable estimate of that phase can be determined by determining the phase of another channel. Since the clock channel has a periodically changing signal, the phase of which can be accurately determined, the clock channel can be used as the best alternative guess of the phase of a data channel in which the data is static. Another data channel would provide a suitable alternative if it had edges in its data signal frequently enough or, as a further alternative, a clock signal derived from an average phase of the channels could be used.

[00012] The longer the period of time since the previous data transition on a given data channel, the less accurate the phase of the data of that channel will be known, since there will not have been an opportunity to adjust the phase in the intervening time. Eventually, the phase of that channel will be so uncertain, that it would be more accurate, the inventors propose,

to use the phase of another channel, preferably the clock channel, as that is likely to be closer to the phase of the given data channel than the phase of the given data channel on its previous data transition.

[00013] It would be possible to simply jump from the last known phase of the data channel to the current phase of the clock channel at the time at which the phase of the clock channel is judged probably to be more accurate than the previous known phase of the data channel.

[00014] An alternative solution is to wait until a suitable time has expired without any data transitions of the data channel and to then move (or "nudge") the phase of the data channel by a small amount around the phase wheel in the direction of the phase of the clock channel. This approach has the advantage of not significantly changing the estimated phase of the data channel by a large amount initially; rather the phase is moved in small increments reflecting the gradual transition from confidence in the phase of the channel to confidence in the phase of, for example, the clock channel. The jitter between channels has random and system components which result from board trace difference among the channels. The ideal transition time is zero providing phase re-alignment.

[00015] The present invention provides a circuit comprising:

[00016] a first data channel and at least one other channel;

[00017] clock synchronising means for generating a local clock synchronised with the first data channel;

[00018] timing means associated with the first data channel for measuring the time since the last data transition on that channel and operable to provide a timing signal indicative of that time;

[00019] phase detect means, associated with the first data channel, for detecting a representative phase of a selected set of one or more channels, that set comprising, at least, said at least one other channel;

[00020] phase adjustment means for adjusting the phase of the local clock in response to the timing signal towards said phase of said set.

[00021] In one arrangement, said set consists of a single channel, being the or one of said at least one other channel, and said representative phase is the phase of that single channel.

[00022] In an alternative arrangement, said set comprises a plurality of channels.

[00023] Preferably, said phase representative of said set is an average of the phases of the members of said set.

[00024] Preferably, said set comprises said at least one other channel and said first data channel itself.

[00025] Preferably, the timing means is arranged to issue a first interval signal when a first time period has elapsed since a last data transition occurred on the first data channel.

[00026] In one arrangement, in the continued absence of a data transition on the first data channel, the timing means is arranged to issue interval signals at constant intervals.

[00027]

In an alternative arrangement, in the continued absence of a data transition on the first data channel, the timing means is arranged to issue interval signals at intervals that get progressively shorter.

[00028]

Preferably, when the intervals get progressively shorter, the intervals are subject to a minimum time interval.

[00029] Preferably, when interval signals are issued, the phase adjustment means is responsive to said interval signals to adjust the phase of the local clock towards the phase of said selected set.

[00030] In one arrangement, the phase adjustment means is responsive to successive interval signals to adjust the phase of the local clock by a constant amount.

[00031] In an alternative arrangement, the phase adjustment means is responsive to successive interval signals to adjust the phase of the local clock by increasing amounts.

[00032] In a further alternative arrangement, the phase adjustment means is responsive to successive interval signals to adjust the phase of the local clock by reducing amounts.

[00033] In one more alternative arrangement, the phase adjustment means is responsive to successive interval signals to adjust the phase of the local clock by initially increasing then by reducing amounts.

[00034]

Preferably, the timing means comprises a counter.

[00035] Preferably, the timing means is so arranged that the counter counts through a number of counts before issuing a timing signal.

[00036] Preferably, the timing means is so arranged that the counter begins a new count each time it issues a timing signal.

[00037] Preferably, the timing circuit is so arranged that each time a timing signal is issued, since the last data transition, the counter counts a respective number of counts in response to being loaded with a respective value stored in the circuit.

Preferably, when the counter begins a new count each time it issues a timing signal, the timing circuit is so arranged that the successive counts are smaller by a constant ratio to the previous one.

[00038] Preferably, the timing circuit is so arranged that after a certain number of successive counts the count becomes constant.

[00039] Preferably, the circuit includes an edge detect circuit for detecting a data transition on the first data channel and resetting in response the sequence of counts.

[00040] Preferably, the circuit includes an edge detect circuit for detecting a data transition on the first data channel and resetting in response the timing means.

[00041] Preferably, the circuit includes an edge detect circuit for detecting a data transition on the first data channel and resetting in response the phase of the local clock to that of the first data channel.

[00042] Preferably, the circuit so operates that the amount of the phase adjustments depends on the magnitude of the difference between the phase of the first data channel and said representative phase of said set.

[00043] The invention also provides a method of providing a local clock signal associated with a first data channel, the method comprising the steps of:

generating a local clock signal synchronised with the first data channel;

measuring the time since the last data transition on the first data channel and providing a timing signal indicative of that time;

detecting a phase representative of a selected set of one or more channels, that set comprising at least one channel other than the first data channel;

adjusting the phase of the local clock, in response to the timing signal, towards the phase of said set.

[00044]
In one method, said set consists of a single channel, that single channel being one of the channels other than the first data channel, and said representative phase is the phase of that single channel.

[00045] In an alternative method, said set comprises a plurality of channels.

[00046] In a method wherein said set comprises a plurality of channels, said phase representative of said set is an average of the phases of the members of said set.

[00047] Preferably, in a method wherein said set comprises a plurality of channels, said set includes said first data channel.

[00048] Preferably, providing said timing signal comprises issuing a first interval signal when a first time period has elapsed since a last data transition occurred on the first data channel.

[00049] In one method, providing said timing signal comprises issuing, in the continued absence of a data transition on the first data channel, interval signals at constant intervals.

[00050] In an alternative method, providing said timing signal comprises issuing, in the continued absence of a data transition on the first data channel, interval signals at intervals that get progressively shorter.

[00051] Preferably, the interval between successive interval signals gets smaller by a constant ratio and, preferably, the intervals are subject to a minimum time interval.

[00052] Preferably, the step of adjusting the phase of the local clock occurs in response to said interval signals.

[00053] In one method, the adjustment of the phase of the local clock occurs in constant amounts.

[00054] In an alternative method, the adjustment of the phase of the local clock occurs in increasing amounts.

[00055] In another alternative method, the adjustment of the phase of the local clock occurs in reducing amounts.

[00056] In a further alternative method, the adjustment of the phase of the local clock occurs initially in increasing amounts and then in reducing amounts.

[00057] Preferably, the method further comprises the step of resetting the phase of the local clock to the phase of the first data channel in response to a data transition on that channel.

[00058] Preferably, the amount of the adjustments of the phase of the local clock depends on the magnitude of the difference between the phase of the first data channel and said representative phase of said set.

BRIEF DESCRIPTION OF THE DRAWINGS

[00059] An embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings, of which:

[00060] FIGURE 1 shows a known differential driver that takes a differential signal and coverts it into a single-ended serial data stream;

[00061] FIGURE 2 shows a data stream generated by the circuit of Figure 1 and an associated clock signal;

[00062] FIGURE 3 shows a phase-locked loop generating multiple phase clock signals from a single reference clock source;

[00063] FIGURE 4 shows a phase wheel;

[00064] FIGURE 5 is a circuit demonstrating a method of obtaining an optimum clock signal;

[00065] FIGURE 6 is a circuit diagram of one implementation of a nudge function in accordance with a first embodiment of the present invention;

[00066] FIGURE 7 is a diagram of a circuit to generate a local clock signal in accordance with the present invention;

[00067] FIGURE 8 is a timing diagram illustrating the functionality of the circuit of Figure 6;

[00068] FIGURE 9 is a timing diagram of a second embodiment of the present invention;

[00069] FIGURE 10 is a circuit diagram implementing the functionality shown in the timing diagram of Figure 9.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[00070] Figure 6 shows a circuit that can be used to implement the nudge function described above. The circuit includes flip-

flops 12 and 14, exclusive-OR (XOR) gate 16 and counter 18. Flip-flops 12 and 14 and XOR gate 16 are used as an edge detector. The data signal of the relevant data channel is coupled to the D-input of flip-flop 12 and the Q-output of flip-flop 12 is coupled to the D-input of flip-flop 14. The Q-outputs of flip-flops 12 and 14 are respectively coupled to first and second inputs of XOR gate 16, the clock inputs of flip-flops 12 and 14 and counter 18 are coupled to a CLK input and the output of the XOR gate provides an EDGE signal, which is coupled to the reset input R of the counter. The counter is provided with an overflow output O so that each time the counter overflows, a nudge signal is provided.

[00071] The CLK input may be a bit-clock, both positive and negative edges being used or, alternatively, a double-rate clock, only positive edges being used.

[00072] The nudge signal produced by the circuit of Figure 6 is used to adjust the phase of the data channel using the circuit of Figure 7. The circuit of Figure 7 uses the PLL 5, phase detector 9 and phase interpolator 10 of Figure 5. In addition, the circuit of Figure 7 includes multiplexer 19, phase selectors 20 and 23, phase detector 21, comparator 22, phase interpolator 24 and PLL 25.

[00073] Phase detector 9 compares the phase output of the phase interpolator 10 and the phase of the data channel and outputs and up/down signal U/D indicative of whether the phase of the data channel is advanced or retarded with respect to the phase output of the phase interpolator. The U/D signal is passed to

multiplexer 19, the select input of which is coupled to the NUDGE output of Figure 6. In the absence of a NUDGE signal (i.e. during the normal mode when data transitions are occurring on the data channel), the U/D signal is passed to phase selector 20. Phase selector 20 advances or retards the phase of the local clock signal and passes that phase information to phase interpolator 10.

[00074] Phase interpolator 10 generates the local clock signal in the same manner as described in relation to Figure 5.

[00075] The clock channel also has a phase detector 21, a phase selector 23, a phase interpolator 24 and a PLL 25. These also function in the same manner as described in relation to Figure 5 to provide a clock signal in phase with the clock channel (with respect to the same reference clock as used for the data channel).

[00076] The output of phase selector 20 for the data channel is also passed to a first input of comparator 22. The second input of comparator 22 is coupled to the output of phase selector 23 for the clock channel. Thus comparator 22 detects whether the phase of the local clock is advanced or retarded with respect to the phase of the clock channel. The output of comparator 22 is provided as the second input to multiplexer 19.

[00077] When a nudge signal is provided at the control input of multiplexer 19, the signal passed to phase selector 20 is the output of comparator 22. Thus a signal indicating whether the local clock is advanced or retarded with respect to the phase of

the clock channel is passed to the phase selector. The phase selector then adjusts the phase of the local clock by a small interval in the direction of the phase of the clock channel, as required.

[00078] The operation of the circuit of Figure 6 is shown in the timing diagram of Figure 8. The output of XOR gate 16 is low when the Q-outputs of flip-flops 12 and 14 are at the same value and high when they are at different values. Thus on each data transition, XOR gate 18 produces a pulse as the effect of that data transition passes through the flip-flop circuits. A number of such pulses are shown at 24, 25, 26, 27 and 28 in Figure 7.

[00079] With each pulse from XOR gate 16, counter 18 is reset to zero. The counter then ramps again towards an overflow amount. When the gap between the reset pulses is sufficiently large to allow the counter to reach the overflow value before a reset pulse is received, a nudge pulse is obtained, for example at points 30, 32, 33 and 34. When a nudge pulse is provided, the counter is reset to zero.

[00080] The change in phase produced by each nudge pulse is constant and the intervals between the nudge pulses 32, 33 and 34 are the same. The phase is simply nudged towards the clock in fixed intervals and when it reaches the phase of the clock channel, the phase simply oscillates either side of the clock phase. A constant phase change for each nudge pulse is the preferred arrangement.

[00081] In the embodiment of the invention shown in Figures 6 and 8, the counter is reset to zero each time a nudge signal is provided. The counter then starts counting again so that, if the data is static for an extended period of time, a succession of nudge signals will be obtained (see, for example, nudge signals 33 and 34), thereby moving the local clock phase towards the phase of the clock channel. Each nudge signal is spaced from the previous nudge signal by a constant period of time: that time period being determined by the clock frequency and the overflow value of the counter.

[00082] It is advantageous to increase the rate at which the phase of the data channel is nudged towards the phase of the clock channel as the time since the last data transition increases. Thus it is advantageous to adapt the reset function of the counter to allow the time between successive nudge signals to get progressively shorter, as shown in the timing diagram of Figure 9.

[00083] In the example of Figure 9, when a data transition occurs, the counter is reset to zero, as before as can be seen at point 35. However, on reaching the overflow amount for a first time, the counter is reset to N/2 (N being the overflow value). On reaching the overflow amount for a second time, the counter is reset to 3N/4, for the third time to 7N/8 and for the fourth time to 15N/16. Thus a nudge signal is generated more and more often as the time since the last data transition increases.

[00084] In the example of Figure 9, once the counter is reset to 15N/16, each successive nudge signal also causes a reset to 15N/16.

[00085] The functionality of the timing diagram of Figure 9 can be achieved using the circuit of Figure 10. The circuit of Figure 10 is a modified version of the circuit of Figure 6 and like circuit elements are labelled with like numerals. The circuit of Figure 10 differs from that of Figure 6 by the addition of a preset circuit 36 and the provision of a modified counter 38 in place of counter 18. Preset circuit 34 has a reset input R coupled to the EDGE signal, a change preset value input CPV coupled to an overflow output O of counter 38 and an output providing a preset value PV input to counter 38.

[00086] Counter 38 differs from that of counter 18 in that, when an overflow condition is detected so that a nudge signal is output from the counter, that nudge signal is provided as a preset input P to the counter. On receiving such a preset input, the counter is preset to the value on the preset value PV input.

[00087] When a data transition is detected by flip-flops 12 and 14 and XOR gate 16, an EDGE signal is applied to both reset circuit 36 and counter 38. That edge signal resets the counter 38 to zero and sets the preset value in preset circuit 36 to N/2. If the overflow condition is reached, the nudge signal forces the preset input P high and the counter value is set to N/2. In addition, the nudge signal is provided as a change present value input CPV to preset circuit 36. In response to this, preset circuit 36 changes the preset value to 3N/4. On the next nudge

signal, the preset value is set to 7N/8 and a further nudge signal sets the preset value to 15N/16. Further nudge signals at this stage do not affect the preset value, which remains at 15N/16. An EDGE signal at any time resets the counter to zero and the preset value to N/2.

[00088] In alternative embodiments of the invention, the change in phase caused by a nudge signal may not be constant. For example, the nudge size could be dependent on the length of time since the last data transition, on the difference in the current phase value of the data stream and the phase value of the clock channel or on a combination of the two.

[00089] The nudge size could be increased with time in order to accelerate the move towards the phase value of the clock rate. This could be used instead of, or in combination with, the increase in frequency of the nudge signals. Alternatively, it may be advantageous to reduce the nudge size with time since, as the phase value gets closer to the phase value of the clock channel, it will not be necessary to change the phase value by much; such a reduction in nudge size would reduce the amount of oscillation of the phase value about the phase value of the clock channel after very long periods without any data transitions. Yet a further embodiment may provide a nudge size that initially increases to accelerate the move towards the phase value of the clock rate and then decreases to reduce the effect of oscillation.

[00090] Instead of varying the preset value to which the counter is preset after a nudge signal is issued, a similar

functionality could be achieved by resetting the counter to zero and varying the value at which the overflow output of the counter is set (i.e. by varying that value at which the nudge signal is issued). The nudge signal could be issued, for example, at a value N for the first time and then at N/2, N/4, N/8 and N/16 for the second, third, fourth and fifth time, respectively. The nudge signal may then be issued at N/16 thereafter.

[00091] In the above examples the phase of the bit clock of the data channel has been nudged towards the phase of a clock channel. It is not necessary that that channel is a clock channel per se. Some other channel that can be relied on in that it has a phase that is close enough to the particular data channel and has a sufficient frequency of edges could be used instead. In a system having several data channels, the channel to be used as a clock channel could be dynamically selected on the basis that it has had edges recently. Further the phase towards which the bit clock of the data channel is nudged could be a phase representative of a plurality channels, for example an average of the phase values provided by respective phase selectors for the plurality of channels. The average need not exclude the channel being nudged which is convenient if several channels are being nudged since the same average can be used for all.